IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PRIORITY Application Serial No. 08/996,325
PRIORITY Filing Date ....December 22, 1997
Inventor ....H. Montgomery Manning
Assignee ....Micron Technology, Inc.
PRIORITY Group Art Unit 2822
PRIORITY Examiner ....M. Trinh
Attorney's Docket No. MI22-1698
Title: Methods of Forming Thin Film Transistors

PRELIMINARY AMENDMENT BEING FILED WITH A DIVISIONAL APPLICATION

To: Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

From: Bernard Berman (Tel. 509-624-4276; Fax 509-838-3424)
Wells, St. John, Roberts, Gregory & Matkin P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828

09920979.080101

Sir:

Please enter the following amendments prior to examining the above-identified application.

AMENDMENTS

In the Specification

At p. 1, before the "Technical Field" section insert:

-- **RELATED PATENT DATA**

This patent is a divisional application of U.S. Patent Application Serial No. 08/996,325 which was filed on December 22, 1997, which is a continuation application of U.S. Patent Application Serial No. 08/506,084, filed July 24, 1995 which is now U.S. Patent No. 5,700,727. --

In the Claims

Please replace the claims with the following clean version of the entire set of pending claims, in accordance with 37 C.F.R. § 1.121(c)(1)(i). Cancel all previous versions of any pending claim.

Add New Claims 69-93 as follows:

69. (New) A thin film transistor comprising:

a variable thickness thin film transistor layer, the transistor layer having a channel region and one of a source region or a drain region elevationally above the channel region, the one region comprising at least a portion thicker than the channel region; and

a gate in lateral proximity to the thin film channel region, the gate comprising an annulus which laterally encircles the laterally proximate thin film channel region.

70. (New) The thin film transistor of Claim 69, the one region and the channel region being elongated, where the channel region is oriented substantially perpendicularly relative to the one region.

71. (New) The thin film transistor of Claim 69, the source region and the drain region being oriented parallel relative to one another, the channel region being oriented substantially perpendicularly relative to both the source and drain regions.

72. (New) The thin film transistor of Claim 69, the source region and the drain region being provided in different elevational planes, the channel region being disposed elevationally between the source region and drain region.

73. (New) The thin film transistor of Claim 72, the source region and the drain region having different thicknesses.

74. (New) The thin film transistor of Claim 69, the channel region comprising an annulus encircled by the gate.

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75. (New) The thin film transistor of Claim 69, further comprising:

a first dielectric layer disposed over a semiconductor substrate;

a gate electrode layer disposed over the first dielectric layer;

a second dielectric layer disposed over the gate electrode layer and having an upper surface; and

an opening extending through the second dielectric layer, the gate electrode layer and the first dielectric layer, the opening, in cross-sectional view, having opposing sidewalls and a bottom disposed between the opposing sidewalls.

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76. (New) The thin film transistor of Claim 75, the variable thickness thin film layer being disposed within the opening and extending outward from the opening and overlying at least a portion of the upper surface.

77. (New) The thin film transistor of Claim 75, at least some of the one region disposed over the upper surface and being thicker than the channel region.

78. (New) The thin film transistor of Claim 75, further comprising a gate dielectric layer within the opening, at least a portion of the gate dielectric layer, in cross-sectional view, being elevationally coincident gate electrode layer.

79. (New) A thin film transistor comprising:

a variable thickness thin film transistor layer, the transistor layer having a thin film channel region, a first thin film source/drain (S/D) region and a second thin film S/D region, the first S/D region having a different thickness than the second S/D region; and

a gate in lateral proximity to the thin film channel region, the gate comprising an annulus which laterally encircles the laterally proximate thin film channel region.

80. (New) The thin film transistor of Claim 79, one of the first thin film S/D region and the second thin film S/D region being disposed elevationally above the thin film channel region, where the one region is thicker than the thin film channel region.

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81. (New) The thin film transistor of Claim 80, the one region and the thin film channel region being elongated, and where the thin film channel region is oriented substantially perpendicularly relative to the one region.

82. (New) The thin film transistor of Claim 79, the first thin film S/D region and the second thin film S/D region being oriented parallel relative to one another, the thin film channel region being oriented substantially perpendicularly relative to both the first and second thin film S/D regions.

83. (New) The thin film transistor of Claim 79, the first thin film S/D region and the second thin film S/D region being provided in different elevational planes, the channel region being disposed elevationally between the first and second thin film S/D regions.

84. (New) The thin film transistor of Claim 79, one of the first thin film S/D region and the second thin film S/D region being provided elevationally above the other of the first thin film S/D region and the second thin film S/D region, the one region being thicker than the other region.

85. (New) The thin film transistor of Claim 79, further comprising:

a first dielectric layer disposed over a semiconductor substrate;

a gate layer disposed over the first dielectric layer;

a second dielectric layer disposed over the gate layer and having an upper surface; and

an opening extending through the second dielectric layer, the gate layer and the first dielectric layer, the opening, in cross-sectional view, having opposing sidewalls and a bottom disposed between the opposing sidewalls, the thin film transistor being disposed within the opening and over the upper surface.

86. (New) The thin film transistor of Claim 85, one of the first thin film S/D region and the second thin film S/D region being provided having at least a portion overlying the upper surface and the other of the first thin film S/D region and the second thin film S/D region being provided having at least a portion overlying the bottom of the opening, the one region being thicker than the other region.

87. (New) The thin film transistor of Claim 85, further comprising a gate dielectric layer disposed within the opening adjacent the opposing sidewalls, where the thin film transistor layer is disposed over the gate dielectric layer.

88. (New) The thin film transistor of Claim 87, the gate dielectric layer being an annulus received in the opening, the annulus having a top disposed elevationally below the upper surface.

89. (New) A thin film transistor comprising:

a first dielectric layer disposed over a semiconductor substrate;

a gate electrode layer disposed over the first dielectric layer;

a second dielectric layer disposed over the gate electrode layer and having an upper surface;

an opening extending from the upper surface to the semiconductor substrate, the opening, in cross-sectional view, having opposing sidewalls;

a gate dielectric layer disposed over a portion of the sidewalls as an annulus, the annulus having a top disposed elevationally below the upper surface; and

a channel region disposed within the opening, operably adjacent the gate dielectric layer.

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90. (New) The thin film transistor of Claim 89, further comprising one of a first diffusion region and a second diffusion region disposed over the upper surface and the channel region.

91. (New) The thin film transistor of Claim 89, further comprising one of a first diffusion region and a second diffusion region disposed over the upper surface and the channel region and the other of the first diffusion region and the second diffusion region disposed elevationally below the channel region.

92. (New) The thin film transistor of Claim 74, wherein the channel region essentially fills the opening.

93. (New) The thin film transistor of Claim 74, wherein the channel region essentially fills the opening and further comprising one of a first diffusion region and a second diffusion region disposed over the upper surface and the channel region and the other of the first diffusion region and the second diffusion region disposed elevationally below the channel region.

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REMARKS

Claims 1-68 are cancelled, and Claims 69-93 are added. It necessarily follows, therefore, that Claims 68-93 are pending in the application. Applicant respectfully requests examination of such pending claims.

Respectfully submitted,

Dated: Aug 1, 2001

By: Bernard Berman
Bernard Berman
Reg. No. 37,279

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VERSION WITH MARKINGS TO SHOW CHANGES MADE IN THE PRELIMINARY AMENDMENT

SPECIFICATION

The specification has been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

At p. 1, before the "Technical Field" section insert:

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CLAIMS

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

Cancel Claims 1-68.

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